Lower Protrusion of a Copper-Nickel Alloy in a Through-Silicon via and Its Numerical Simulation

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The application of Cu-filled through-silicon via (TSV) in 3-D integrated circuit packaging faces several fabrication and reliability issues. In this study, we introduced a Cu-Ni alloy for TSV filling with a high filling speed and a reduced TSV protrusion. In particular, the characteristics of Cu-Ni via protrusions at various annealing temperatures (~200–450°C) were investigated with experimental and numerical analysis and compared with Cu-filled vias. High speed Cu-Ni alloy filling into the vias was achieved without any defects by an electroplating process that used a periodic pulse reverse current waveform. The Cu-Ni alloy TSV showed lower via protrusion than the Cu TSV. The simulated protrusion heights of the Cu-Ni vias were in good agreement with the experimental results. The simulation results also indicated that the Cu-Ni TSVs has smaller protrusions than the Cu TSVs. As the annealing temperature was varied from 200 to 450°C, the protrusions increased gradually and became significant at an annealing temperature of 350°C. When the temperature was increased further, the protrusions became larger due to severe creep deformation. The von Mises stress also increased with increasing annealing temperature, and increased substantially at a temperature of 300°C due to the creep effect. In summary, the Cu-Ni alloy TSVs showed smaller protrusions relative to the Cu TSVs. The stress level of the Cu-Ni via was lower than that of the Cu via. These results indicate that the Cu-Ni alloy TSV had advantages in terms of high speed filling and smaller protrusions, demonstrating its promise as an alternative to current Cu TSV technologies.


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1. Introduction

Although through-silicon vias (TSVs) have great potential to be used in 3-D IC packaging, there are still many problems to overcome in order to achieve mass production with low cost. In general, TSV technologies utilize copper (Cu)-filling by the electroplating method due to the good electrical properties and easy processing of Cu. However, Cu-filling still faces several reliability and manufacturability issues. Firstly, the coefficient of thermal expansion (CTE) of copper (~17.5 × 10^-6/°C) is much higher than that of silicon (~2.5 × 10^-6/°C) and the surrounding dielectric materials. As a result, copper expands five to six times more than silicon during high temperature fabrication or environmental temperature cycling. The thermo-mechanical stress caused by this CTE mismatch results in several reliability concerns such as interfacial delamination, cracking, voiding, and TSV protrusion. Cu protrusions in TSVs, also known as Cu pumping and Cu extrusion, have been discussed recently in the literature. During the fabrication of TSVs, the vias undergo thermal annealing at up to ~450°C with metallization and/or bonding processes at ~250°C. At any high temperature step of the TSV manufacturing process, the copper, which is confined in the via hole, will expand in the vertical direction and subsequently extrude out of the Si wafer surface (due to its higher CTE). Cu protrusion can lead to cracking or delamination of the overlying dielectric and/or metal layers. Since Cu protrusion is a critical problem in the back-end-of-line (BEOL) process, several studies have been conducted to characterize and alleviate this phenomenon using experimental and numerical simulation methods. It has been determined that Cu protrusion is not fully-reversible and that localized plastic deformation plays an important role in TSV protrusion. Optimization of the annealing conditions is known to be an important factor to avoid further plastic deformation of copper in the vias. Secondly, Cu-filling of the vias normally takes a long time (~approximately 15 h), and defects are most likely to occur at longer filling times. These long processing times represent a huge drawback for the commercial realization of TSV technologies. To reduce the Cu-filling time, a pulse-reverse (PR) current waveform (modified from the pulse current) or the addition of inhibitors and accelerators to the plating solution have been reported.

As a fundamental solution to overcome these problems, several recent studies have looked into replacing copper with different filling materials, such as tungsten, polymers, alloys, and solders, in an attempt to reduce the thermo-mechanical stress and shorten the Cu-filling time. He et al. suggested a Cu-cored solder for rapid and low-cost processing for TSV fabrication. Ko et al. introduced a vacuum-assisted via filling method with a molten solder. They reported that the filling time for vias with a diameter of 30 µm was only 0.5 s, which was substantially faster compared to conventional electroplating methods. In the authors’ previous study, we demonstrated a high speed Cu-Ni alloy filling method into TSVs where a periodic pulse reverse (PPR) current waveform was applied to reduce the filling time of the electroplating. Although several alternative filling materials are suggested, little attention has been paid to Cu protrusions and limited information about this subject is currently available. In this study, we investigated the characteristics of TSV protrusions for high speed Cu-Ni alloy filling in comparison with Cu-filling. TSV protrusions at various annealing temperatures were experimentally characterized. Finite element analysis (FEA) simulations were also used to investigate TSV protrusion behavior.
2. Experimental Procedure

To fabricate the TSV structure, a (100) p-type Si wafer (100 mm in diameter and 525 µm in thickness) was used as a substrate. A photo resist (PR, AZ4620) was spin-coated to produce via holes on the wafer surface. Subsequently, the wafer was etched by the deep reactive ion etching (DRIE) method. An array of TSVs (30-µm diameter, 200-µm pitch, and 60-µm depth) was fabricated. Each 5 mm x 5 mm wafer was composed of 240 chips, and 256 vias were prepared in each chip. A SiO2 layer with a thickness of 1 µm was formed as an insulation layer by the plasma enhanced chemical vapor deposition (PECVD). Ti (300 nm) and Au (500 nm) layers were sputtered in the via walls as adhesion and seed layers, respectively. The Si wafer was cut into chips with a diamond saw. The diced chips were used as the cathode for Cu-filling by electroplating, and a Pt sheet (size: 10 mm x 10 mm x 0.3 mm) was used as the anode. A commercial pulse-plating unit (EPP-4000 from Princeton Applied Research) was used as the power supply for electroplating. The reference electrode for electroplating was a standard calomel electrode (SCE). The electroplating solution for Cu-Ni filling was composed of 150~200 g/l of CuSO4, 150~200 g/l of NiSO4, 32 ml/l of H2SO4, and additives. The electrolyte in the plating bath was stirred continuously by a magnetic bar at 200 rpm (revolutions per minute), and the electrolyte was kept at room temperature during electroplating. The schematic diagram for the experimental setup is shown in Fig. 1. A periodic pulse reverse current was used to avoid high concentrations of ions in the opening region of the via. Therefore, the ion concentration is homogenized throughout the via, and clogging of the via opening is prevented during the application of the pulse (reduction) current. A more detailed fabrication procedure is explained in Ref. 20).

After filling the Cu-Ni alloy into the via, any Cu-Ni overflow on top of the wafer surface was removed by the chemical mechanical polishing (CMP) process. The Cu-Ni filled TSV wafer was annealed at a high temperature, ranging from 200°C to 450°C, using a vacuum furnace. The heating rate was maintained at 5°C/min for an annealing duration of 30 min. Cu-Ni alloy-filled vias were observed by field emission scanning electron microscopy (FE-SEM, Hitachi-S4300) to investigate the filling ratio of the vias and to observe the deposition morphology. Cu-Ni TSV protrusions were measured with atomic force microscopy (AFM). An electron probe micro analyzer (EPMA, JEOL JXA-8500F) was used to investigate the elemental analysis of the filled Cu-Ni alloy vias.

3. Results and Discussions

Figure 2 shows SEM images of the via protrusion shapes for the Cu-Ni TSVs with annealing temperature ranging from 200°C to 450°C. The SEM images show that the protrusion height increases with the annealing temperature. In order to...
precisely measure the protrusion height of the extruded Cu-Ni TSV. AFM was used. Figure 3 shows AFM images of the protruded vias for each annealing temperature. Via protrusions begin to be visually observable at the annealing temperature of 300°C. Figure 4 shows a plot of the maximum protrusion height as a function of annealing temperature. It is clear that the protrusion height increases with annealing temperature. The protrusion height at 300°C is 260 nm, which is a relatively small protrusion. Protrusions start to increase substantially at 350°C. At an annealing temperature of 450°C, the protrusion height increases to 1250 nm. To compare the protrusion amount of Cu-Ni filled TSVs with that of conventional Cu-filled TSVs, we fabricated Cu-filled TSVs separately and measured their protrusion height at 450°C. The protrusion height of the Cu TSV at an annealing temperature of 450°C was 1360 nm (solid rectangular symbol in Fig. 4), which showed a higher value than that of the Cu-Ni TSV. We did not measure the change in the Cu protrusion height at various annealing temperatures because there have already been several reports detailing the measurements of Cu TSV protrusions.\(^{5,6,9}\) It is clear that the Cu-Ni TSV shows lower via protrusion than the conventional Cu TSV. However, a protrusion height of 1.25 µm is still high enough to cause fracture of the overlying BEOL layer. The values of the protrusion heights in this study are actually relatively larger than those reported in previous studies.\(^{5,6,9}\) This is caused by the fact that the via diameter in our study is larger than those in previous studies; previous researchers used smaller vias with diameters less than 10 µm. It is well known that Cu protrusion from TSVs increases with increasing via diameters. Larger vias will result in larger protrusions due to the larger Cu volume.\(^7\) Therefore, we expect that the protrusion height will decrease if we reduce the via diameter.

The Cu-Ni alloy samples were observed by FE-SEM to investigate the filling ratio of the vias and to observe the deposition morphology. Furthermore, the EPMA was used to investigate the elemental analysis of the filled Cu-Ni alloy TSVs. Figure 5 presents SEM images and EPMA mappings for cross-sections of the Cu-Ni filled vias. SEM analysis showed that a complete filling ratio was achieved without serious defects or voids. Even after aging this sample at 450°C for 30 min, an interfacial delamination or a crack at the interface between the Cu-Ni alloy in TSV and SiO\(_2\) insulation layer was not observed. Using FE-SEM images, the Cu-filling ratio was measured by the commercial program, Carl Zeiss Zxiovision. In the EPMA analysis, Cu and Ni exhibited a nearly identical distribution across the via hole. EPMA results indicated that the composition of the Cu-Ni alloy via consisted of 92 mass% Cu and 8 mass% Ni. The uniform distribution of Cu and Ni in the Cu-Ni alloy via did not change with increasing annealing temperature.

In this paper, finite element analysis was used to investigate Cu-Ni TSV protrusions. Figure 6 shows a geometrical schematic diagram of the TSV structure. The isolated blind TSV was modeled, and quarter symmetric FEA models were adopted for computational efficiency. The silicon substrate is 70 µm in thickness and 80 µm square. The diameter and depth of the TSV are 30 µm and 60 µm, respectively. The thickness of the silicon oxide barrier layer is 1 µm. Figure 7 shows the quarter symmetric FEM modeling of the Cu-Ni TSV structure. The symmetric boundary condition was applied onto two vertical cutting sides of the structure, and one node at the origin of global coordinate system was additionally constrained for the x, y, and z axes.

FEAs of Cu-Ni TSV protrusions were conducted at various annealing temperatures. In simulation, the elastic-plastic behaviors of Cu and Cu-Ni alloy are not sufficient to predict the protrusion behavior at high temperatures due to creep effects. It is well known that copper will creep at a high fraction (\(>0.4\)) of its melting temperature (1083°C). Therefore, it is thought that Cu or Cu-Ni alloy could creep under annealing temperatures above 300°C. Therefore, in this study, elastic-creep properties were used to consider the creep behavior of Cu and Cu-Ni alloy. The other materials were regarded elastic materials. Table 1 shows the material properties used in the FEM simulation.\(^{7,21,22}\) Since the material properties of 92 mass% Cu and 8 mass% Ni alloy material did not exist in any literatures, we used an effective modulus concept in approximate calculation of elastic Young’s modulus and CTE. The rule of mixture was applied to calculate the effective material properties.\(^{23}\) The rule of mixture is constructed by two parameters namely the modulus and the volume fraction of each component of the material. For Cu and Cu-Ni alloy, the time dependent creep properties was used. The time hardening implicit creep equations with ANSYS FEA software were used in this study. For the simulation of Cu and Cu-Ni alloy creep, we used the common creep relation of eq. (1) with a creep strain rate (\(\dot{\epsilon}_{cr}\)), applied stress (\(\sigma\)), temperature (\(T\)), and time (\(t\)):

\[
\dot{\epsilon}_{cr} = A \exp \left( -\frac{Q}{RT} \right) \sigma^n \epsilon^m
\]

where \(n\) and \(m\) are the stress- and time-hardening exponents, respectively. \(Q\) is the activation energy in kJ mol\(^{-1}\), \(R\) (8.314 J mol\(^{-1}\) K\(^{-1}\)) is the universal gas constant, and \(A\) is a constant. Creep constants of Cu were referenced from the existing literature.\(^7\) For copper, the material constant \(A = 1.43 \times 10^{10}\), \(Q = 197 kJ mol^{-1}\), \(n = 2.5\), and \(m = -0.9\). For Cu-Ni alloy material, the creep constant of 92 mass% Cu and 8 mass% Ni alloy material did not exist in any literatures. Only available Cu-Ni alloy material in existing literatures, which has similar composition of 92 mass% Cu and 8 mass% Ni alloy, was 97.6 mass% Cu-2.2 mass% Ni-0.2 mass% Be alloy material.\(^{24}\) Therefore, we used the creep constants of 97.6% Cu-2.2% Ni-0.2% Be alloy material for creep simulation of the Cu-Ni alloy TSV. For Cu-Ni alloy, the creep constant \(A\) is 1.07 \(\times\) \(10^9\), \(Q = 197 kJ mol^{-1}\), \(n = 2.5\), and \(m = -0.75\). The room temperature (25°C) condition is assumed to be a stress-free condition where all materials in the TSV structure remain without any deformation. In order to simulate the actual annealing process, the numerical simulation was conducted in three steps. Firstly, the temperature was increased from room temperature (25°C) to the annealing temperature (200–450°C) (ramp up step). Secondly, the temperature was held at the annealing temperature (200–450°C) for 30 min at creep strain effect conditions (dwelling step). As a final annealing step, the TSV structure was cooled down to room temperature (25°C). TSV protrusion simulation results were obtained at the final annealing step at which TSV was cooled down to room temperature.
Fig. 3  AFM images of Cu-Ni filled via protrusions at various annealing conditions: (a) 200°C, (b) 250°C, (c) 300°C, (d) 350°C, (e) 400°C, and (f) 450°C.

Fig. 4  AFM measurement results of Cu-Ni via protrusions with increasing annealing temperature compared with Cu via protrusions.

Fig. 5  EPMA mapping results of Cu-Ni filling by PPR current waveform with various annealing temperatures: (a) 200°C, (b) 300°C, (c) 400°C, and (d) 450°C.

Fig. 6  Schematic drawing of the TSV structure used in the FEA study.
FEM analyses were conducted with various annealing temperatures ranging from 200°C to 450°C and compared with the experimental results. Figure 8 shows cross-sectional views of the simulated Cu and Cu-Ni TSV deformations for various annealing temperatures; the displacements in the z-direction have been exaggerated by a factor of two times for better visualization. It can be clearly seen that Cu-Ni protrudes out of the vias in the vertical direction when the temperature is increased to different annealing temperatures. The Cu-Ni TSV showed less protrusion than Cu TSV. Figure 9 shows the simulated Cu-Ni TSV protrusion heights in comparison with the experimentally measured data. The Cu-Ni via protrusion increases with increasing annealing

![Figure 8](image1)

![Figure 9](image2)

### Table 1 Material properties used in this study.

<table>
<thead>
<tr>
<th>Material</th>
<th>Young's modulus (GPa)</th>
<th>Poison's ratio ((\nu))</th>
<th>CTE (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>131</td>
<td>0.28</td>
<td>2.8</td>
</tr>
<tr>
<td>SiO(_2)</td>
<td>73</td>
<td>0.17</td>
<td>0.5</td>
</tr>
<tr>
<td>Cu</td>
<td>91.7</td>
<td>0.34</td>
<td>17.6</td>
</tr>
<tr>
<td>Cu-Ni alloy</td>
<td>95</td>
<td>0.34</td>
<td>17.4</td>
</tr>
</tbody>
</table>
temperature. The results of the simulated Cu-Ni via protrusion heights are relatively in good agreement with the experimentally measured data. The difference between the experimental results and simulation results could be attributed to the material properties used in the simulation such as creep constants as well as the experimental measurement errors. To compare the protrusions of the Cu-Ni TSV with the Cu TSV, the Cu TSV protrusion was also simulated using FEM. Figure 10 shows the summary of the experimental and simulation results of Cu-Ni and Cu via protrusion height. The simulated maximum protrusion heights at 450°C for the Cu-Ni and Cu TSV were 1.94 and 2.11 µm, respectively. As shown in Fig. 10, both the experimental and simulation results indicate that the amount of protrusion of the Cu-Ni TSV is smaller than the Cu TSV. The protrusion evolution behavior of the Cu-Ni TSV, with increasing annealing temperature, is nearly identical with that of the Cu TSV. As the annealing temperature increases, Cu is expanded vertically because it is constrained by the surrounding Si substrate. Due to the thermal expansion (CTE) mismatch between Cu (≈16.7 ppm/°C) and the Si substrate (≈2.3 ppm/°C), thermal stresses build up inside the TSV when it is subjected to thermal treatment.\(^3\)\(^,\)\(^7\) During the annealing process, irreversible deformation or plastic deformation occurs when the thermal stress in the Cu TSV is greater than the elastic limit of Cu. When the annealing temperature is above 350°C, protrusions become larger because of the large Cu creep deformation. Due to the irreversible creep deformation of copper, protruding Cu can never return to its original position when the TSV is cooled down to room temperature. Smaller protrusion of Cu-Ni TSV than Cu TSV might be attributed to a higher melting temperature of nickel composition, which is 1455°C.

Figure 11 shows the typical von Mises stress distribution of the cross-section of the Cu-Ni TSV structure with increasing temperature. (a) Ram up to an annealing temperature of 300°C, (b) dwelling for 30 min at 300°C, (c) ramp down from 300°C to room temperature.
Figure 13 shows the simulation results of the maximum von Mises stress in the Cu-Ni via and the Cu via after cooling down to room temperature with increasing annealing temperature. The maximum stress increases with increasing annealing temperature. In particular, the maximum stress increases sharply at a temperature of 300°C possibly owing to the creep effect of via material. Higher annealing temperature generates larger creep deformation of Cu-Ni and Cu TSV via, which is irreversible deformation and thus results in larger stress when temperature changes from annealing temperature to room temperature. At a higher annealing temperature, the stress increased slightly due to the softening effect of the Cu and Cu-Ni via material. In general, the Cu-Ni via exhibited lower stress level than the Cu via structure, however, the differences in stress level become small from 350°C. At an annealing temperature of 300°C, the Cu-Ni via expanded vertically due to the CTE mismatch between the via and the surrounding materials. When the temperature increased to above 350°C, protrusions became larger due to increased Cu creep deformation. The von Mises stress in the Cu-Ni via increased with increasing annealing temperature, and increased substantially at a temperature of 300°C due to the creep effect of via material. Overall, the Cu-Ni alloy TSV showed high speed filling and a lower via protrusion. This indicates that Cu-Ni alloy vias represent a promising alternative to Cu vias for TSV technologies.

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REFERENCES