Thermoelectric Power-Generation Characteristics of a Thin-Film Device Processed by the Flip-Chip Bonding of Bi$_2$Te$_3$ and Sb$_2$Te$_3$ Thin-Film Legs Using an Anisotropic Conductive Adhesive

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A thermoelectric thin-film device with a cross-plane configuration was fabricated by the flip-chip process using an anisotropic conductive adhesive. The Cu/Au bumps on the top substrate were flip-chip bonded to the 242 pairs of the n-type Bi$_2$Te$_3$ and p-type Sb$_2$Te$_3$ thin-film legs electrodeposited on the bottom substrate. The internal resistance of the thin-film device was 59Ω, most of which can be attributed to the interfacial resistance of the 484 flip-chip joints. The thin-film device exhibited an open-circuit voltage of 382 mV and a maximum output power of 652 µW for a temperature difference of 36.8 K applied across its top and bottom substrates. [doi:10.2320/matertrans.M2015236]

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Keywords: thermoelectric device, thin film, bismuth telluride, antimony telluride, electrodeposition, flip chip, anisotropic conductive adhesive

1. Introduction

With the low power consumption of electronic devices, micro energy harvesting has been extensively investigated to provide micro power sources for wearable electronics, wireless sensor networks (WSN), and body area networks (BAN), as well as autonomous and stand-alone health-monitoring devices for machine, industrial and civil structures.1-7 Various energy sources, such as vibration/motion, indoor and outdoor light, and thermal energy, are available ambiently.8 Thermoelectric thin-film devices have great potential as micro generators for ambient energy harvesting because they can be operated with minor temperature differences produced by small heat sources, such as body heat. Thermoelectric thin-film devices also have various advantages, such as high power density, long lifetimes and high reliability with no moving parts.1,9,10

A thermoelectric thin-film device can be classified as having either an in-plane (planar) or cross-plane configuration based on the direction of the heat flow through the device.7,11 Compared to an in-plane thin-film device, a cross-plane device is more suitable for power-generation applications because of its low electrical resistance and lack of parasitic heat flow through the substrate.7-12 While a thermoelectric thin-film device of the cross-plane configuration has various processing difficulties, such as the long deposition time to form thick thermoelectric films and the formation of electrodes on its substrates,8,10 bonding of the metal bumps in the top substrate to the thermoelectric thin-films in the bottom substrate is a critical factor for the power-generation characteristics of the thin-film device.7,9

In this work, we fabricated a thermoelectric thin-film device of the cross-plane configuration by flip-chip bonding of the upper electrodes to the electrodeposited n-type Bi$_2$Te$_3$ and p-type Sb$_2$Te$_3$ thin-film legs. With its advantages in fabricating semiconductor packages of thin thickness, light weight, small size, and high density and fine pitch interconnection, flip-chip bonding has been extensively investigated in the microelectronic packaging industry in recent years to mount a semiconductor chip directly to a substrate.12,13 We characterized the thermoelectric power-generation characteristics of the thin-film device by applying various temperature differences across its hot and cold ends.

2. Experimental Procedure

The fabrication steps for the bottom substrate consisting of the thermoelectric thin-film couples and the top substrate consisting of the Cu/Au bumps before their flip-chip bonding are illustrated in Figs. 1 and 2, respectively. A Si wafer was used as the bottom and top substrates of the thin-film device because of its thermal conductivity of 148 W/mK, which is high among nonmetals.14 For insulation, a 100-nm-thick SiO$_2$ layer was formed on the surface of the Si wafer by dry

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oxidation. In Figs. 1 and 2, we denoted the Si wafer with a 100-nm-thick SiO₂ layer on its surface as just the Si wafer for simplicity.

To form the thin-film legs in the bottom Si substrate, 0.1-μm-thick Ti and 2-μm-thick Cu were sequentially sputtered onto a Si wafer as a seed-layer for electrodeposition of the p-type Sb₂Te₃ and n-type Bi₂Te₃ thin-film legs, as illustrated in Fig. 1(a). After forming a photoresist (PR) pattern to electrodeposit the Cu/Au electrodes of 110 μm × 390 μm in size, 10-μm-thick Cu and 0.1-μm-thick Au were sequentially electrodeposited to form the bottom Cu/Au electrodes, as illustrated in Fig. 1(b). After PR patterning to create 100-μm-diameter holes, the p-type Sb₂Te₃ thin-film legs with a thickness of 20 μm were electrodeposited in an aqueous solution containing 70-mM Sb-Te electrolytes with an Sb/(Sb + Te) mole fraction of 0.9 at a constant current density of 1.25 mA/cm², as illustrated in Fig. 1(c). Another PR pattern was formed to create 100-μm-diameter holes, and the 20-μm-thick n-type Bi₂Te₃ thin-film legs were electrodeposited in a nitric-acid aqueous solution containing 50-mM Bi-Te with a Bi/(Bi + Te) mole fraction of 0.5 in 1 M of HNO₃ at a constant current density of 12.5 mA/cm², as illustrated in Fig. 1(d). Mechanical polishing was performed on the over-electrodeposited Sb₂Te₃ and Bi₂Te₃ thin-film legs in the PR template to obtain a smooth and flat surface as well as a uniform height of 7 μm. After PR patterning to open the top surfaces of the Bi₂Te₃ and Sb₂Te₃ thin-film legs, 2-μm-thick Ni and 2-μm-thick Au were sequentially electrodeposited to form the capping layer on the Bi₂Te₃ and Sb₂Te₃ thin-film legs, as illustrated in Fig. 1(e). After subsequent PR patterning, the Ti/Cu metatllization except the area underneath the Cu/Au electrodes was removed by etching in a 10% HF solution, as shown in Fig. 1(f).

To form the top Si substrate with the Cu/Au bonding bumps, 0.1-μm-thick Ti and 2-μm-thick Cu were sequentially sputtered onto a Si wafer as a seed layer for electrodeposition of the Cu/Au electrodes and the Cu/Au bonding bumps, as shown in Fig. 2(a). After PR patterning to form the surfaces of the Bi₂Te₃ and Sb₂Te₃ thin-film legs, 2-μm-thick Ni and 2-μm-thick Cu were sequentially electrodeposited to form the Bi₂Te₃ and Sb₂Te₃ thin-film legs, as illustrated in Fig. 2(b). After another PR patterning to create 85-μm-diameter holes, 10-μm-thick Cu and 2-μm-thick Au were sequentially electrodeposited to form the Cu/Au bumps, as illustrated in Fig. 2(c). After subsequent PR patterning, the Ti/Cu metallization except the area underneath the Cu/Au electrodes was removed by etching in a 10% HF solution, as shown in Fig. 2(d).

To bond the Cu/Au bumps of the top Si substrate to the Ni/Cu caps on the Bi₂Te₃ and Sb₂Te₃ thin-film legs of the bottom Si substrate, an ACA (anisotropic conductive adhesive: Fujikura Kasei Co., LTD. Type LS210FP3) was dispensed on the bottom substrate. Then, the Cu/Au bumps of the top substrate were aligned and flip-chip bonded to the thin-film legs of the bottom substrate by curing the ACA at 160°C for 30 sec with a bonding pressure of 52 MPa, forming the thin-film device consisting of 242 pairs of the Bi₂Te₃ and Sb₂Te₃ thin-film legs, as schematically illustrated in Fig. 3. As schematically illustrated in Fig. 4, the conductive particle in the ACA was made of a polymer sphere electrodeposited with a thin Ni layer for electrical conduction and subsequently coated with a thin polymer layer for insulation. During flip-chip bonding, the conductive particles entrapped between the Cu/Au bumps of the top substrate and the Ni/Au caps on the thin-film legs of the bottom substrate were compressed and changed shape from spherical to oval with wearing and breaking of the thin insulating polymer layer on the Ni coating of the conductive particles. This phenomenon resulted in electrical connection in the z-direction through the Ni layer coated on the polymer sphere between the upper Cu/Au bonding bump and the lower Ni/Au cap.

The Seebeck coefficient (α) of the electrodeposited Bi₂Te₃ and Sb₂Te₃ thin films of 20 μm in thickness was measured at room temperature by applying a temperature difference of 20°C at both ends of the film. The electrical resistivity (ρ) of the Bi₂Te₃ and Sb₂Te₃ films was measured using the four-point-probe method, and the power factor (P) was evaluated using the relation \[ P = \alpha^2 / \rho \]. Power generation characteristics, such as the output voltage and the output power, of the thin-film device were measured by placing the device between an electrically heated copper heat source and a water-cooled copper heat sink. The apparent temperature difference \( \Delta T \) applied across the top and bottom substrate of the thin-film device was measured using thin k-type thermocouples placed between the thin-film device and the heat source/sink surfaces.

3. Results and Discussion

Table 1 lists the compositions and thermoelectric properties of the electrodeposited Bi₂Te₃ and Sb₂Te₃ films of 20 μm in thickness. Details on the crystal structures and thermoelectric properties of the electrodeposited Bi₂Te₃ and Sb₂Te₃ films can be found elsewhere. Cross-sectional scanning electron micrographs of the thin-film device, shown in Fig. 5, reveal that electrical contacts between the Cu/Au bumps of the top substrate and the Ni/Au caps on the thin-film legs of the bottom substrate were accomplished via the conductive
particles in the ACA, which were trapped and compressed into an oval shape between them.\textsuperscript{15,16} While the contact resistance of the flip-chip interfaces depends on the number of conductive particles entrapped at the interfaces, it would be easier to increase the number of entrapped conductive particles by changing the ACA to one containing more conductive particles rather than by modifying the process with the same ACA. A flip-chip process using solder reflow or an adhesive anisotropic conductive paste of solder particles\textsuperscript{17,18} can be applied to reduce the contact resistance by forming more contact area between the Cu/Au bumps and the Ni/Au caps on the thin-film legs.

Figure 6 illustrates the output voltage-current characteristics of the thin-film device at a temperature difference $\Delta T$ ranging from 6 K to 36.8 K applied across its top and bottom substrates. From the slopes of the output voltage-current curves, the average internal resistance $R_G$ of the thin-film device was measured to be 59 $\Omega$. The dependence of the open-circuit voltage $V_{oc}$ on the apparent temperature difference $\Delta T$ across the thin-film device is shown in Fig. 7. The open-circuit voltage exhibited a linear increase with increasing $\Delta T$, reaching 382 mV at a $\Delta T$ of 36.8 K. The slope of the open-circuit voltage versus the temperature difference $\Delta T$ is 8.85 mV/K, which is much smaller than the 132 mV/K estimated for the 242 pairs of Bi$_2$Te$_3$-Sb$_2$Te$_3$ legs using the Seebeck coefficients of the Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films listed in Table 1. The open-circuit voltage $V_{oc}$ of a thermoelectric generator is expressed as $V_{oc} = n\alpha \Delta T_G$, where $n$ is the number of p–n leg couples, $\alpha$ is the summed Seebeck coefficient of a p–n couple, and $\Delta T_G$ is the actual temperature difference working across the thermoelectric thin-film legs.\textsuperscript{7–9,11,19} Comparison of the measured Seebeck coefficient for the thin-film device, 8.85 mV/K, with the estimated value of 132 mV/K suggests that the actual temperature difference $\Delta T_G$ across the thin-film legs is approximately 1/15 of the apparent temperature difference $\Delta T$ applied across the top and bottom substrates of the thin-film device. For a $\Delta T$ of 36.8 K, the actual temperature difference $\Delta T_G$ could be 2.5 K.

<table>
<thead>
<tr>
<th>Film</th>
<th>Bi or Sb Composition (at%)</th>
<th>Seebeck Coefficient (µV/K)</th>
<th>Electrical Resistivity ($\times 10^{-5}$ Ω m)</th>
<th>Power factor ($\times 10^{-4}$ W/m·K$^2$)</th>
</tr>
</thead>
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<tr>
<td>Bi$_2$Te$_3$</td>
<td>40</td>
<td>$-60$</td>
<td>0.7</td>
<td>5.1</td>
</tr>
<tr>
<td>Sb$_2$Te$_3$</td>
<td>43</td>
<td>485</td>
<td>4.8</td>
<td>49.0</td>
</tr>
</tbody>
</table>

Fig. 5 Cross-sectional scanning electron micrographs of the thin-film device of (a) low magnification and (b) high magnification showing the conductive particles deformed to an oval shape between the Cu/Au bump and the Ni/Au cap.

Fig. 6 Output voltage-current curves of the thin-film device measured at various apparent temperature differences applied across its top and bottom substrates.

Fig. 7 Open-circuit voltage vs. the apparent temperature difference applied across the top and bottom substrates of the thin-film device.
The internal resistance $R_G$ of the thin-film device is the sum of the material resistance $R_m$ and the interfacial resistance of the flip-chip joints $R_i$. The material resistance $R_m$ is comprised of the resistances of the Bi$_2$Te$_3$ legs, the Sb$_2$Te$_3$ legs, and the Ni/Au capping layers on the thin-film legs in the bottom substrate and the Cu/Au bumps in the top substrate, as well as the Ti/Cu/Au electrodes in the bottom and top substrates. The interfacial resistance $R_i$ is the resistance arising at the flip-chip bonded interfaces between the Cu/Au bumps of the top substrate and the Ni/Au capping layers on the thin-film legs of the bottom substrate. Using the resistivities of the Bi$_2$Te$_3$ and Sb$_2$Te$_3$ thin films listed in Table 1 with the resistivities of 2.35 × 10$^{-8}$ Ω·m, 1.67 × 10$^{-8}$ Ω·m, 44 × 10$^{-8}$ Ω·m, and 6.84 × 10$^{-8}$ Ω·m for Au, Cu, Ti, and Ni, respectively,20,21 the material resistance $R_m$ was calculated to be 14 Ω. By subtracting the material resistance $R_m$ from the internal resistance $R_G$ of 59 Ω, the interfacial resistance $R_i$ was evaluated as being 45 Ω. As the thin-film device contains 484 flip-chip joints, the average contact resistance $R_c$ of one flip-chip joint is 93 mΩ. A wide range of average contact resistances, from 1 mΩ to a few hundred mΩ, has been reported for semiconductor packages processed by flip-chip bonding with ACA or ACF (anisotropic conductive film).15,16,22-25) The contact resistance of a flip-chip joint has been found to depend upon the ACA conducting materials and their density, bonding parameters such as the bonding temperature and pressure, and bonding tracks such as the structure and materials of chip bumps and substrate pads.15,16,22-25)

From the device configuration shown in Fig. 3, the equivalent thermal circuit for the thin-film device can be depicted as in Fig. 8, and the total thermal resistance $\theta_{total}$ of the thin-film device can be expressed as eq. (1), where $\theta_{module}$ is the thermal resistance of the module and $\theta_{ACA}$ is the thermal resistance of the entire ACA filling the module. Then, the thermal resistance of the module $\theta_{module}$ can be expressed as eq. (2), where $\theta_p$ is the thermal resistance of the top Si substrate of 5.4 mm × 6.4 mm in size and 550 μm in width with 100-nm-thick SiO$_2$ on its top and bottom surfaces, $\theta_p$ is the thermal resistance of the 242 Ti/Cu/Au electrode pads on the top substrate, $\theta_b$ is the thermal resistance of the 484 flip-chip bonded interfaces, $\theta_i$ is the thermal resistance of the 424 pairs of Bi$_2$Te$_3$-Sb$_2$Te$_3$ thin-film legs with the Ni/Au capping layers on them, $\theta_{bp}$ is the thermal resistance of the 242 bottom Ti/Cu/Au electrode pads, and $\theta_{bs}$ is the thermal resistance of the bottom Si substrate of 12 mm × 11 mm × 550 μm in size with 100-nm-thick SiO$_2$ on its top and bottom surfaces.

$$1/\theta_{total} = 1/\theta_{module} + 1/\theta_{ACA}$$  \hspace{1cm} (1)

$$\theta_{module} = \theta_o + \theta_p + \theta_b + \theta_i + \theta_G$$
$$+ \theta_{bp} + \theta_{bs} \approx \theta_i + \theta_G$$  \hspace{1cm} (2)

Using the thermal conductivities of 148 W/m·K, 1.4 W/m·K, 31 W/m·K, 483 W/m·K, 345 W/m·K, 158 W/m·K, 1.2 W/K, and 1.02 W/m·K reported for Si, SiO$_2$, Ti, Cu, Au, Ni, Bi$_2$Te$_3$, and Sb$_2$Te$_3$, respectively,14,26,27) the thermal resistances of $\theta_o$, $\theta_p$, $\theta_b$, $\theta_i$, $\theta_{bp}$, and $\theta_{bs}$ were calculated to be 0.11 K/W, 0.003 K/W, 0.01 K/W, 1.67 K/W, 0.002 K/W, and 0.03 K/W, respectively. As the values of $\theta_o$, $\theta_p$, $\theta_b$, $\theta_i$, $\theta_{bp}$, and $\theta_{bs}$ are quite small relative to $\theta_i$, the thermal resistance of the module $\theta_{module}$ could be simplified as the sum of $\theta_i$ and $\theta_G$ in eq. (1).

The relation between the Seebeck coefficient $\alpha_m$ actually measured for the thin-film device and the Seebeck coefficient $\alpha_e$ estimated for the thin-film device with the thermoelectric characteristics of the Bi$_2$Te$_3$ and Sb$_2$Te$_3$ thin films in Table 1 can be expressed as eq. (3). By substituting 8.85 mV/K for $\alpha_m$, 132 mV/K for $\alpha_e$, and 1.67 K/W for $\theta_G$, the interfacial thermal resistance $\theta_i$ of the 484 flip-chip bonded joints could be estimated as 23.2 K/W.

$$\alpha_m = \frac{\theta_G}{\theta_{module}} \alpha_e \approx \frac{\theta_G}{\theta_i + \theta_G} \alpha_e$$  \hspace{1cm} (3)

As the interfacial resistance of a flip-chip joint is based on the metal-metal contact between the Cu/Au bumps, the Ni coating of the conductive particles, and the Au/Ni capping layer, the thermal contact resistance $\theta_i$ of each flip-chip joint can be related to its contact resistance $R_c$ using the Wiedemann-Franz law as eq. (4), where $L_o$ is the Lorenz constant.28)

$$\theta_i = \frac{R_c}{L_o T}$$  \hspace{1cm} (4)

By substituting 93 mΩ for $R_c$, 2.44 × 10$^{-8}$ W/K$^2$ for $L_o$,26) and 300 K for $T$, the thermal contact resistance $\theta_i$ of each flip-chip joint was estimated to be 12,707 K/W. In our device configuration shown in Fig. 3, the 484 flip-chip joints were connected thermally in parallel. Thus, the total interfacial thermal resistance, $\theta_i$, of the 484 flip-chip joints could be evaluated as 26.3 K/W, which is in excellent agreement with the 23.2 K/W estimated above using eq. (3) for the relation between $\alpha_m$ and $\alpha_e$.

The output power-current characteristics of the thin-film device at various apparent temperature differences $\Delta T$ are plotted in Fig. 9. The maximum output powers of 652 μW, 221 μW, 71 μW, and 9 μW were obtained at a $\Delta T$ of 36.8 K, 24.7 K, 17 K, and 6 K, respectively. A maximum output power $P_o$ of a thermoelectric device at an actual temperature difference $\Delta T_G$ across the thin-film legs can be expressed by eq. (5), where $n$ is the number of p-n couples; $\alpha$ and $\rho$ are the combined Seebeck coefficient and resistivity of the p-type and n-type thin films, respectively; and $d$ and $t$ are the diameter and thickness of the thin-film legs, respectively.9,20) As given in eq. (5), the maximum output power $P_o$ can be enhanced by reducing the internal resistance $R_G$ by adopting more conductive electrodes and improving the
flip-chip process. As shown in Fig. 9, the thin-film device exhibited a maximum output power of 221 µW at a ΔT of 24.7 K, which was much higher than the 6 µW at a ΔT of 22.3 K reported for the thin-film device having the high internal resistance of 3.7 kΩ. Substituting the maximum output voltage $V_{oc}$ of 230 mV at a ΔT of 24.7 K and the internal resistance $R_G$ of 59 Ω into eq. (5) yields the maximum output power of 224 µW for the present thin-film device, which is in excellent agreement with the measured value of 221 µW. The thin-film device having the internal resistance of 3.7 kΩ exhibited a $V_{oc}$ of 294 mV at a ΔT of 22.3 K. A maximum output power of 8 µW is estimated using eq. (5), which is also well matched to the value of 6 µW obtained by measurement for this device.

$$P_o = \frac{V_{oc}^2}{4R_G} = \frac{(n\alpha)^2\Delta T_G^2}{4R_G} \approx \frac{n\alpha^2}{16\rho L} \cdot n \cdot d^2 \cdot \Delta T_G^2 \quad (5)$$

A maximum output power $P_o$ can be optimized by adjusting the geometry of the thin-film legs for the given thermoelectric materials. As controlling the thickness of a thin-film leg in a wide range is much more difficult than its diameter, let us consider how the maximum output power changes with the diameter of the thin-film legs at a fixed thickness. The internal resistance $R_G$ of 59 Ω was the sum of the material resistance $R_m$ of 14 Ω and the flip-chip interfacial resistance $R_i$ of 45 Ω. As most of the material resistance $R_m$ arises from the Bi$_2$Te$_3$ and Sb$_2$Te$_3$ thin-film legs (12 Ω out of 14 Ω) and the interfacial resistance $R_i$ depends on the cross-sectional area of the flip-chip joints, the internal resistance $R_G$ is inversely proportional to the square of the thin-film leg diameter. Consequently, the maximum output power $P_o$ is proportional to the square of the thin-film leg diameter, as given in eq. (5). Increasing the diameter of the thin-film legs in a substrate of fixed area will lead to a decrease in the number $n$ of p-n thin-film couples. If the distance between the Bi$_2$Te$_3$ and Sb$_2$Te$_3$ legs is adjusted proportionally to the thin-film leg diameter, the increase in the cross-sectional area of the complete set of thin-film legs will be completely compensated by the decrease in the number of thin-film couples. Then, the maximum output power $P_o$ will not be changed by varying the thin-film leg diameter. However, the distance between a Bi$_2$Te$_3$ leg and a Sb$_2$Te$_3$ leg does not need to be increased proportionally to the leg diameter and can instead be kept to a certain minimum, which is appropriate for device processing, regardless of the leg diameter. In this case, the increment in the cross-sectional area of thin-film legs ΔA will always prevail over the decrement of the leg-pair number $Δn$, resulting in an increase in the maximum output power $P_o$ for increasing leg diameter $d$. As implied by eq. (3), the relation between the apparent temperature difference $ΔT$ and the actual temperature difference $ΔT_G$ depends on the ratio of $\theta_i$ to $\theta_G + \theta_i$. Thermal resistances of both the thin-film legs $\theta_G$ and the flip-chip interfaces $\theta_i$ decrease in the same manner when increasing the cross-sectional area of thin-film legs at a fixed thickness, such that the actual temperature difference $ΔT_G$ will not be affected by changing the leg diameter. While the maximum output power $P_o$ increases when increasing the leg diameter $d$, the open circuit voltage $V_{oc}$ drops when increasing the leg diameter $d$ because of the decrease in the number of p-n couples. Thus, the leg diameter must be determined by considering the optimization of both the output power and the voltage characteristics of the thin-film device.

4. Conclusion

A thermoelectric thin film device of the cross-plane configuration was fabricated by flip-chip bonding of the Cu/Au bumps in the top Si substrate to the 242 pairs of the n-type Bi$_2$Te$_3$ and p-type Sb$_2$Te$_3$ thin-film legs in the bottom Si substrate. From the slopes of the output voltage-current curves, the internal resistance of the thin-film device was evaluated as being 59 Ω, which was comprised of the material resistance 14 Ω and the flip-chip interface resistance 45 Ω. Due to the large thermal resistance of the flip-chip bonded interface, the actual working temperature difference across the thin-film legs was substantially reduced to approximately 1/15 of the apparent temperature difference applied across the top and bottom substrates of the thin-film device. The output power of the thin-film device is strongly dependent upon its internal resistance. Compared to the 6 µW at a ΔT of 22.3 K obtained for a thin-film device with a high internal resistance of 3.7 kΩ, a large maximum output power of 221 µW was generated at a ΔT of 24.7 K for the thin-film device with a low internal resistance of 59 Ω. With the difficulty of forming thermoelectric thin films with large thicknesses, controlling the diameter of the thermoelectric thin films would be useful to optimize both the output power and the output voltage characteristics of the thin-film device.

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